In Re Patent Application of:
MARINET ET AL.
Serial No. 10/004,527
Filing Date: November 1, 2001

REMARKS

Applicants appreciate the Examiner's careful and thorough examination of the present application, and for correctly withdrawing the previous rejection in view of the arguments presented in Applicants' response. By this amendment, various claims have been amended to further clarify the invention. Claims 23-37 have been canceled to further clarify the issues and advance prosecution of the application. Claims 16-22 and 36-45 remain pending in the application. Favorable reconsideration is respectfully requested.

I. The Invention

As shown in FIGS. 1-7, for example, the invention provides additional protection to integrated circuits that handle confidential information, in particular those that are mounted within smart cards. This is achieved by providing a method and/or circuit for protecting an integrated circuit against piracy. After an initialization process of a CPU and before a predetermined processing sequence, the CPU of the integrated circuit detects the state of a timer. The CPU performs the processing sequence and controls the activation of the timer if it is not activated, and the CPU disables the IC if the timer is activated.

II. The Claims are Patentable

Claims 16-45 were rejected in view of Yach et al. (U.S. Patent No. 5,454,114) in view of Green (U.S. Patent No. 4,769,765) or in various combinations with Schrenk (U.S. Patent No. 5,497,462), Sutherland (U.S. Patent No. 6,292,898) and/or Brehmer et al. (U.S. Patent No. 5,563,799) for the

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reasons set forth on pages 2-10 of the Office Action. Applicants contend that Claims 16-22 and 36-45 clearly define over the cited references, and in view of the following remarks, favorable reconsideration of the rejections under 35 U.S.C. §103 is requested.

The independent Claims 16 and 38 each include the CPU of the integrated circuit detecting the state of the timer after performing an initialization sequence but before a processing sequence. If the timer is not activated, the CPU activates the timer and performs the processing sequence. The CPU disables the IC if the timer is activated. It is these combinations of features which is not fairly taught or suggested in the cited references and which patentably define over the cited references.

The Yach et al. patent is directed to a microcontroller, which is adapted, when operating, to execute programs and instructions and, in response, to generate control signals to selectively control an external apparatus. The microcontroller includes a power supply for supplying power to the overall device within a predetermined range suitable for its operation, and a clock for supplying a clock frequency to the microcontroller with a stability suitable for precise timing and counting within the device. The microcontroller is selectively reset to prevent it from executing programs and instructions for purposes of generating the control signals, and is maintained in the reset condition despite initiation of a removal from the reset condition, until the power supplied by the power supply is in a predetermined range and the clock frequency supplied by the clock is stable.

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The portions of the Yach et al. reference relied upon by the Examiner refer to start-up timers, power-up timers and sleep modes. However, nothing in these portions suggests that after an initialization sequence but before a predetermined processing sequence, the CPU of the integrated circuit detects the state of a timer, and controls the activation of the timer if it is not activated, and disables the IC if the timer is activated. Indeed, the microcontroller in Yach et al. is under the control of the power-up and clock timers.

The Green patent is directed to a control system which can be attached to equipment such as appliances or automobiles. The control system includes an enabling/disabling device such as a relay in a circuit in the equipment. A time setting device is used to program a microprocessor with the times when the relay will open and close, thereby disabling and enabling the equipment. The time setting device can only be used to set the times by a person having an authentic authorization device such as a card or a key. The card is read by a card reader and the information obtained is compared by the microprocessor with the authentic information.

The Green reference also does not disclose or teach the use of a CPU of an IC that is under the control of a timer at all, let alone a CPU that disables the IC if a timer is activated when starting a processing sequence after an initialization process. Thus, the Examiner's hypothetical combination of the microcontroller of Yach et al. with the equipment timer of Green, even if obvious, still does not meet the features of the claimed invention.

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Furthermore, the Schrenk patent is directed to a method and circuit for protecting circuit configurations having an electrically programmable non-volatile memory used as a non-volatile counter, an access check is provided in the circuit configuration by comparison of a check code to be fed in with a secret code. The Sutherland and Brehmer et al. references have been relied upon by the Examiner to show various other features such as erasure of data and details of timer circuits. However, none of these references makes up for the deficiencies of the Yach et al. patent and Green patent as discussed above. In other words, the combination of teachings of the various references cannot meet the features of the present invention as claimed.

As the Examiner is aware, to establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the reference itself or in the knowledge generally available to one of ordinary skill in the art, to modify the reference. Second, there must be a reasonable expectation of success. Finally, the prior art reference must teach or suggest all the claim features.

There is simply no teaching or suggestion in the cited references to provide the combination of features as claimed. Accordingly, for at least the reasons given above, Applicants maintain that the cited references do not disclose or fairly suggest the invention as set forth in the independent claims. Furthermore, no proper modification of the teachings of these references could result in the invention as claimed. Thus, the rejections under 35 U.S.C. 103(a) should be withdrawn.

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It is submitted that the independent claims are patentable over the prior art. In view of the patentability of the independent claims, it is submitted that their dependent claims, which recite yet further distinguishing features are also patentable over the cited references for at least the reasons set forth above. Accordingly, these dependent claims require no further discussion herein.

III. Conclusion

In view of the foregoing remarks, it is respectfully submitted that the present application is in condition for allowance. An early notice thereof is earnestly solicited. If, after reviewing this Response, there are any remaining informalities which need to be resolved before the application can be passed to issue, the Examiner is invited and respectfully requested to contact the undersigned by telephone in order to resolve such informalities.

Respectfully submitted,

PAUL J. DITMYER
Reg. No. 40,455
Allen, Dyer, Doppelt, Milbrath & Gilchrist, P.A.
255 S. Orange Avenue, Suite 1401
Orlando, Florida 32802
407-841-2330
Attorney for Applicants